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Triangular Potential Well Approximation in Scaled MOSFET for Low Frequency Noise Modeling and Characterization

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Abstract: *In solid state devices, noise generally come out as current or voltage fluctuations, that can break out from several sources. The intrinsic noise of electronic devices misrepresent many aspects of electronic system development, In this paper, a triangular potential well approximation is presented in scaled MOSFET for $1/f$ low frequency noise modeling and characterization in nano-scaled MOS devices. Noise is a performance feature in generation of electronic devices, noise can serve as a investigative tool to determine important device parameters. The simulation of triangular potential well approximation for quantized energy levels and quasi-Fermi level versus surface potential presents outstanding performance.*

Keywords: *MOSFET, CMOS, Triangular Well Approximation, Low Frequency Noise, Modeling.*

I Introduction

The metal-oxide-semiconductor field-effect transistor (MOSFET) is a type of insulated-gate field-effect transistor that is fabricated by the controlled oxidation of a semiconductor, typically silicon. The voltage of the covered gate determines the electrical conductivity of the device; this ability to change conductivity with the amount of applied voltage can be used for amplifying or switching electronic signals. field-effect transistors (FETs) have a few disadvantages like high drain resistance, moderate input impedance and slower operation. To overcome these disadvantages, the MOSFET which is an advanced FET is invented [1–3].

I-A Construction of MOSFET

The construction of a MOSFET is a bit similar to the FET. An oxide layer is deposited on the substrate to which the gate terminal is connected. This oxide layer acts as an insulator (SiO_2 insulates from the substrate), and hence the MOSFET has another name as IGFET. In the construction of MOSFET, a lightly doped substrate, is diffused with a heavily doped region. Depending upon the substrate used, they are called as P-type and N-type MOSFETs [4–6]. The Figure 1 presents the construction of a MOSFET.

The voltage at gate controls the operation of the MOSFET. In this case, both positive and negative voltages can be applied on the gate as it is insulated from the channel. With negative gate bias voltage, it acts as depletion MOSFET while with positive gate bias voltage it acts as an Enhancement MOSFET [7, 8].

I-B Classification of MOSFETs

Depending upon the type of materials used in the construction, and the type of operation, the MOSFETs are classified as presented in Figure 2. MOSFETs are classified as two modes – enhancement mode and depletion mode. They are futher classified as P-channel and N-channel.

II MOSFET Scaling

Over the past decades, the ongoing MOSFET size scaling results in a great improvement in the integrated circuit operation [9]. The early typical MOSFET channel lengths were several micrometers, but Intel has produced CPUs of 65 nanometer technology with the channel being even shorter than 65 nm in 2006 and in late 2009 Intel began the process featuring 32 nm feature size [10]. With downscaling in size, the process speed of the CPU is boosting, as we have experienced. The

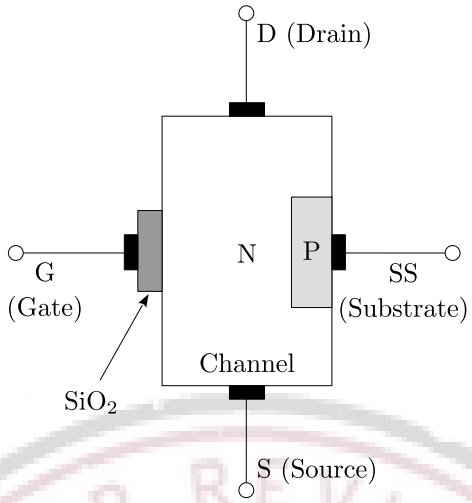

Figure 1: Construction of MOSFET

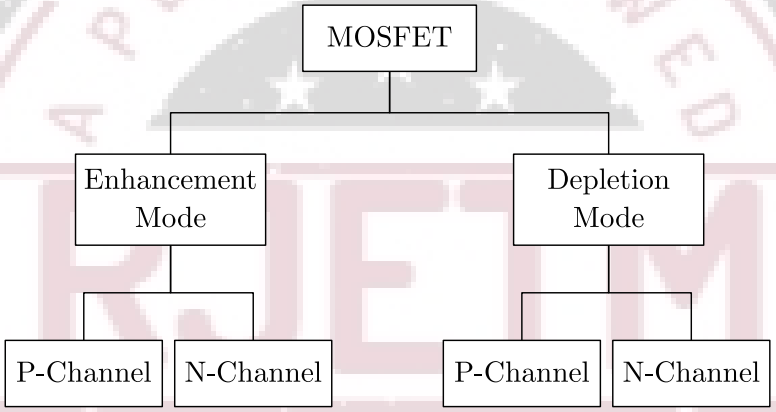

Figure 2: Classification of MOSFETs

main reason to make MOSFET smaller in size is to pack more components on each single chip. High packing density results in realizing the same function in a smaller area and chips with more functionality in the same area [11].

Also, the scaling practice could reduce the price of integrated circuit chips. The cost of fabrication of a piece of wafer is relatively fixed, however the size of each wafer has been increased from 3 inch to 16 inches, and therefore there are more chips that can be fabricated on a single wafer. Therefore, the functions per chip increase. The continuous scaling practice for device and material processes is reaching their limits [12]. The pioneering semiconductor device idea and advanced fabrication technology are required to keep up with the 'roadmap' updated annually by ITRS (International Technology Roadmap for Semiconductor) [13, 14], which describe the forecasts and technology barriers for development. In recent years, other problems have come up as the MOSFETs is scaled down to ¡65 nm. The most straightforward problem is the gate leakage current. In addition to the leakage current, there is another important parameter in MOSFET operation drive current. The drive current is the drain saturation current when MOSFET is working [15, 16]. Using the gradual channel approximation, the drive current is

$$I_{D,sat} = \frac{W}{L}\mu C_{ox}\frac{(V_G - V_T)^2}{2} \tag{1}$$

Where W and L are the width and length of the MOSFET channel, μ is the charge carrier effective mobility, C_{ox} is the gate oxide capacitance and V_G and V_T are gate voltage and threshold voltage. The drive current is required to be considerable enough in order to successfully drive the next level components on the chips. The gate oxide capacitor is similar to a simple parallel-plate capacitor when it is in accumulation, the thin oxide layer leads to a large capacitance and a substantial drive current can be obtained [17]. As discussed above, a thin oxide layer applied in the scaling practice increases the drive current when the MOSFET is on and reduces the sub threshold leakage when the MOSFET is off.

However, because the gate oxide is quite thin, the quantum mechanical phenomenon of the electron tunneling occurs between the gate and the channel. Therefore, a leakage current flows from the semiconductor to the gate metal, passing through the oxide layer [18].

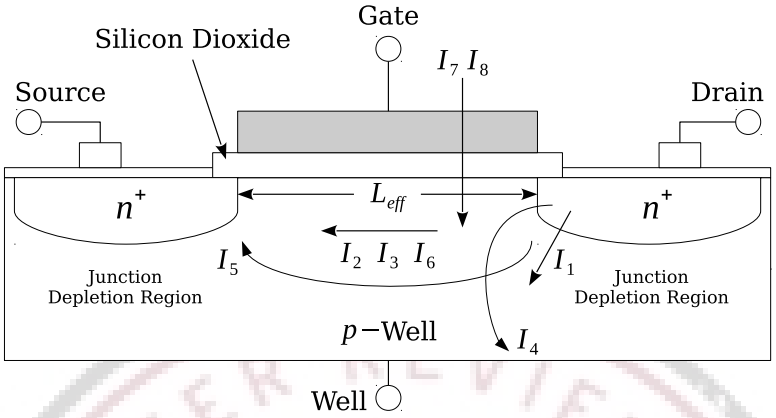

Figure 3: MOSFET Device

As a result, extra power consumption is induced. The ultra thin gate oxide layer in the scaling practice helped improve MOSFET's but also introduced some drawbacks. The major drawback is the large gate leakage current. The ultra thin gate oxide layer leads to high gate oxide capacitance, which is the direct reason for improvement in the drive current and sub threshold leakage [19]. It requires the oxide layer to be electrically thin then the oxide layer can store charges and induce an electric field easily as a great capacitor of high value. On the other hand, the gate leakage current is mainly due to a quantum mechanical tunneling of electrons which has nothing to do with an electrical issue but mainly to do with a wave-particle duality. Therefore, a physical thick layer could function as a barrier for tunneling effectively. Hence, the gate oxide layer has to be electrically thin but physically thick in order to maintain the improvement introduced by an ultra thin oxide and to minimize the tunneling effect as well [20, 21].

MOSFET, the essential building block of very-large-scale integrated (VLSI) circuits, has become the most important microelectronic device [22]. The major development of MOS technology led to the speedy improvement in computer and communication integrated circuits that we have seen in the past decades. The solution to this progression is the 'scaling' in the semiconductor industry which refers to reducing the size of the MOSFET. Small dimensions of each single MOSFET have the advantages of high packaging density, high electronic circuits speed and less power dissipation [23–25].

II-A High$-K$ Gate Dielectric

In order to make the gate oxide layer thick enough to keep electrons from tunneling while inducing an electric field easily to modulate the current in the channel of MOSFETs, it is a straightforward method to use other materials instead of silicon dioxide to build the gate dielectric layer. High$-k$ materials meet the requirements of being electrically thin but thick [26, 27].

The term high$-k$ refers to high dielectric constant. The Equivalent Oxide Thickness (EOT) is an important terminology in high$-k$ field [28], which indicates how thick a silicon oxide layer would need to be in order to produce the same effect as the high-k material being used. The EOT is calculated as the ratio of the dielectric constant of high$-k$ material over that of silicon dioxide [29].

$$\text{EOT} = \frac{\varepsilon_{oxide}}{\varepsilon_k} t_k \tag{2}$$

Where ε_{oxide} and ε_k are the dielectric constants of silicon dioxide and high$-k$ material respectively, and t_k is the physical thickness of the gate layer built with high$-k$ material [30]. The insulator using high$-k$ material could provide a greater capacitance than that of a silicon dioxide layer of the same thickness. The gate insulator of MOSFETs made of high$-k$ material has a relatively greater thickness but quite small EOT, which is the electrical thickness. The high$-k$ materials suitable to be integrated into the MOSFETs require high-quality interface between the high$-k$ material and silicon [31]. The interface quality would affect the charge carrier mobility in the channel directly. Large mobility leads to a high drain current. If the interface has poor quality, there would be more defects and traps, which cause more carriers scattering and subsequently decrease the mobility. Therefore, the interface of great quality is a key consideration. Deposition of high$-k$ dielectric materials directly on silicon results in a very poor interface, which has a large amount of defects [32]. A critical

solution is to form a thin SiO_2 layer (0.5–0.7 nm) before deposition of high$-k$ oxide materials. With this interfacial SiO_2 layer, high-quality interface between high$-k$ oxides and silicon is restored [33, 34].

III Literature Survey

A number of MOSFET circuit designs have been presented by other researchers that make use of or aim to improve the low-frequency noise performance.

III-A Microwave Noise Modeling for MOSFETs

Yu *et al.* [35] proposed a set of new analytical expressions for the noise parameters of MOSFETs in the microwave frequency range. These expressions are derived on the basis of an accurate small-signal and noise model and on an improved small-signal parameter extraction method without any assumptions and approximations. The validity of the new approach is proved by comparison with measured noise parameters up to 14 GHz in a multi-bias region, where a good agreement has been obtained. In the lower gigahertz range, the new expressions can be simplified significantly. Because of the pure analytical nature of the new model, the efficiency of circuit simulation tools can be improved considerably after implementing the equations.

From the circuit point of view, the MOSFET device can be treated as a black box of a noisy two port. As well known, the noise behavior of a linear noisy two-port network can be characterized by the four-noise parameters, $F_{\min}$, R_n, G_{opt} and B_{opt}, with

$$F = F_{\min} + \frac{R_n}{G_S}\left[(G_S - G_{\text{opt}})^2 + (B_S - B_{\text{opt}})^2\right] \tag{3}$$

where F is the noise factor, $Y_S = G_s + jB_S$ is the source admittance, and $Y_{\text{opt}} = G_{\text{opt}} + jB_{\text{opt}}$ is the optimum source admittance.

III-B Low-Frequency Noise Phenomena in Switched MOSFETs

Wel *et al.* [36] tried to give circuit designers some insight into RTS noise phenomena. The common models used in circuit simulators have significant limitations when applied to small-area devices with a low number of free carriers, as the LF noise performance of these devices is dominated by Random Telegraph Signals (RTS).

The observation that in large devices, LF noise decreases when the device is subjected to large signal excitation is explained by the bias dependency of the RTS time constants coupled to the U-shaped distribution of interface states. In small devices, though the noise will go down on average, it is not possible to predict the behavior of each individual device in advance.

For circuit designers, awareness of non-steady-state LF noise phenomena is important because in many circuits, the devices are operated in a switched fashion. Under these conditions, LF noise of the devices will not be the same as during steady-state biasing. In a switched current source, this was shown to result in a significant LF noise reduction. For a correlated double sampling circuit, this means that the bias history for both sample instants must be identical if the noise reduction is to function as intended. For RF circuits where devices are rapidly switched on and off, improved LF noise performance may be expected.

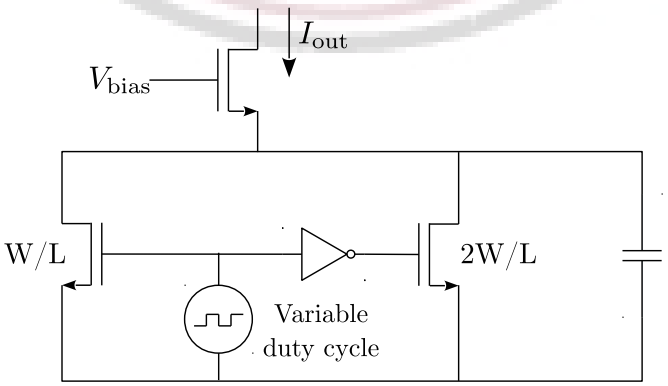

Figure 4: Switched Current Source

III-B.1 Switched Current Source

One example of where classic LF noise modeling clearly shows its limits is the switched current source of Figure 4. This is a current source that alternately activates a transistor with width and one with width. By changing the duty-cycle from 0 to 100% the current can be varied by a factor 2. A filter is placed at the output to suppress the obvious HF fluctuations in current. As an added bonus, the LF noise of the current source decreases when the duty cycle of the driving square wave is not 0 or 100%. This is due to the LF noise of both evices being uncorrelated. The measured LF output noise of the circuit, however, is much lower than predicted by traditional models. This is caused by the decrease of the LF noise of the devices as a result of the large signal square wave they are subjected to.

III-C Low-Frequency Noise Characterization of Germanium n-Channel FinFETs

Oliveira *et al.* [37] confirmed that the carrier number $1/f$ noise also plays a dominant role in Ge n-channel FinFET devices, similar as in planar Ge devices. Moreover, it indicates that the oxide trap density has a lower level than for planar n-/p-channel Ge devices. Finally, the LFN analysis also revealed the uniformity of the trap density in the gate oxide layer and the presence of GR-noise centers in the depletion region.

III-D Modeling of Low Frequency Noise in FD SOI MOSFETs

El Husseini *et al.* [38] showed that when Fully Depleted Silicon On Insulator (FD-SOI) devices are biased in the back conduction regime, the noise behavior is still dominated by the buried oxide noise contribution. Therefore, in this mode of operation, there is no need to consider the impact of the front interface on the device total noise. In a second part of this work, we presented an analytical reformulation of the inversion charge power spectral density valid for the different modes of operation of Fully Depleted Silicon On Insulator (FD-SOI) devices. When the front channel is activated, this analytical model considers the noise contributions of the front and back interfaces.

IV Proposed Approach

The triangular well approximation replaces the potential $\phi(z)$ in Schrödinger and Poisson equations by $F_S \cdot z$ inside the silicon substrate ($z < 0$) and by an infinite barrier in the dielectric ($z > 0$) based on the assumption of a linear shape of the potential in the semiconductor surface layer. This approximation leads to the Airy function with solutions

$$\Psi_{ij} = A_i \left\{ \left(\frac{2m_{i3} q \mathcal{E}_s}{\hbar^2} \right)^{1/3} \left(|z| - \frac{E_{ij}}{q\mathcal{E}_s} \right) \right\} \tag{4}$$

$$E_{ij} = \left(\frac{\hbar^2}{2m_{i3}} \right)^{1/3} \left[\frac{3}{2} \pi q \mathcal{E}_s \left(j + \frac{3}{4} \right) \right]^{2/3} \tag{5}$$

where the surface electric field is

$$\mathcal{E}_s = \frac{q(N_B + N_n)}{\epsilon_s} \tag{6}$$

N_B is the total number of charges per unit area in the depletion layer and N_n is the total number of charges per unit area in the inversion layer.

$$N_n = \sum_{ij} N_{ij} \tag{7}$$

$$N_B = \sqrt{\frac{2\epsilon_s \phi_d (N_A - N_D)}{q}} \tag{8}$$

where ϕ_d is the effective band bending from the bulk to the surface, apart from the contribution of the inversion layer itself, and

$$\phi = \phi_S - \frac{k_B T}{q} - \frac{q N_n z_{av}}{\epsilon_s} \tag{9}$$

z_{av} is the weighted average separation of inversion charge away from the interface, which can be calculated as

$$z_{av} = \sum_{ij} \frac{N_{ij} z_{ij}}{N_n} \tag{10}$$

and z_{ij} is approximated as 2/3 of the distance where the ij th sub-band energy level intercepts the linear potential well, i.e.,

$$z_{ij} = \frac{2E_{ij}}{3q\mathcal{E}_s} \tag{11}$$

Triangular well approximation is easy to solve, if we use the surface field E_s as the unknown variable, the rest of unknowns parameters can be calculated accordingly. The solving process is fast to converge as well, if certain algorithm is utilized.

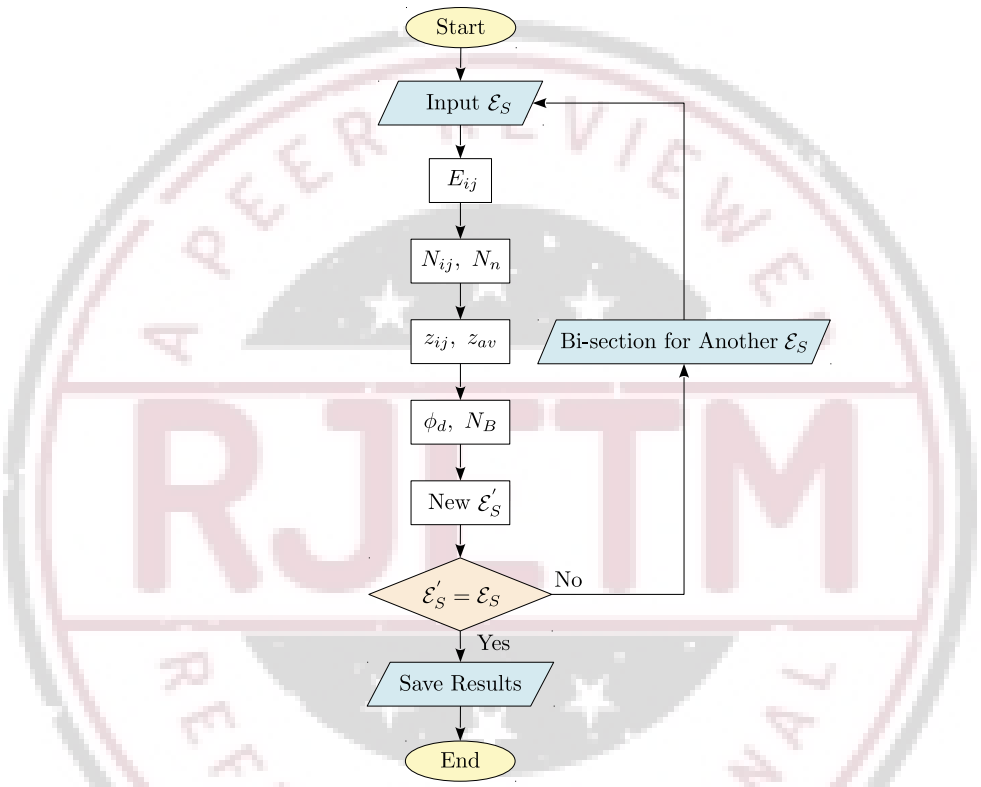

Figure 5: Proposed Triangular Well Flow Chart

For the work presented in this paper, the bi-sectional method is used, with the flow chart shown in Figure 5.

IV-A Variational Approach

The triangular-well is a reasonable approximation when there is little or no charge in the inversion layer, but fails when the charge density per unit area in the inversion layer is comparable to or exceeds that in the depletion layer [49]. Additionally, during the later development of the scattering parameter modeling, this approximation is found to over-simplify the field dependence of the charge separation. Due to these facts, we need to seek another way to construct the sub-band structures. A variational approach gives a good estimate for the energy of the lowest sub-band, when only one sub-band is occupied [49]. This approach also enables us to use the Stern-Howard wave function. For the lowest sub-band, the wave function is

$$\Psi_{00}(z) = \left(\frac{b_i^3}{2}\right)^{1/2} z \exp\left(-\frac{b_i z}{2}\right) \tag{12}$$

where the parameter b_i is determined by minimizing the energy of the system and is given as

$$b_i = \left[\left(\frac{12 m_{i3} q^2}{\epsilon_s \hbar^2}\right)\left(N_B + \frac{11}{32} N_B\right)\right]^{1/3} \tag{13}$$

if the small perturbation term [49] is neglected. The variational results are as follows.

$$z_{00} = \overline{z_{00}} + \delta z_{00} \tag{14}$$

$$\overline{z_{00}} = \left[\frac{9\epsilon_s\hbar^2}{4m_{03}q^2\left(\frac{11}{32}N_n\right)}\right]^{1/3} \tag{15}$$

$$\delta z_{00} = \frac{4N_A\overline{z_{00}}^2}{9\left(\frac{11}{32}N_n\right)} \tag{16}$$

$$E_{00} = \overline{E_{00}} + \delta E_{00} \tag{17}$$

$$\overline{E_{00}} = \left(\frac{3}{2}\right)^{5/3}\left(\frac{q^2\hbar}{\sqrt{m_{03}\epsilon_s}}\right)^{2/3}\left(N_n + \frac{55}{99}N_n\right)\left(N_n + \frac{11}{32}N_n\right)^{-1/3} \tag{18}$$

$$\delta E_{00} = -\left[\frac{2N_Aq^2\overline{z_{00}}^2}{3\epsilon_s\left(N_n + \frac{11}{32}N_n\right)}\right]\left(N_n + \frac{11}{32}N_n\right) \tag{19}$$

Approximate energy levels for the excited states can be obtained in the electric quantum limit by treating the inversion-layer potential and the curvature of the depletion potential as perturbations. The energy levels for the excited states are approximately given by

$$E_{ij} = E_{ij,d} - \frac{q^2\mathcal{E}_B\mathcal{E}_nz_{av}^2}{4E_{ij,d}} - \frac{4E_{ij,d}^2}{15q\mathcal{E}_Bz_d} + q\mathcal{E}_nz_{av} \tag{20}$$

where

$$E_{ij,d} = \left(\frac{\hbar^2}{2m_{i3}}\right)^{1/3}\left[\frac{3}{2}\pi q\mathcal{E}_B\left(j + \frac{3}{4}\right)\right]^{2/3} \tag{21}$$

$$\mathcal{E}_B = \frac{qN_B}{q} \tag{22}$$

$$\mathcal{E}_n = \frac{qN_n}{q} \tag{23}$$

$$z_d = \sqrt{\frac{2\epsilon_s\phi_d}{qN_B}} \tag{24}$$

The second term in the Equation 20 is the approximate lowering of the excited-state energy by the inversion-layer potential well. The third term gives the approximate contribution of the depletion-potential curvature to the energy levels. The last term gives the inversion-layer contribution to the potential energy at the surface.

Unlike the previously mentioned triangular well approximation, where the whole group of expressions can be setup by solving for the surface field F_s, there is more than one key unknown variable (N_B and N_n, at least) in the variational approach. Iteration in 2 directions is quite inefficient. Thus, we decided to use the triangular-well results as a starting point and iterate N_B and N_n around that states for a pair of values which achieve the self-consistency: if we use this pair of N_B and N_n to calculate the subband structures and use these new subband energy levels to obtain another pair of N_B and N_n; when the newly-obtained N_B and N_n roughly agree with the original N_B and N_n, the iteration reaches self-consistency.

V Result Analysis

The simulation result and comparison are included in the following figures. Figure 6 depicts the first three sub-bands energy levels E_{00}, E_{01} and E_{10} as functions of the surface potential ϕ_S. E_{00} is the lowest level, while E_{10} is slightly lower than E_{01}.

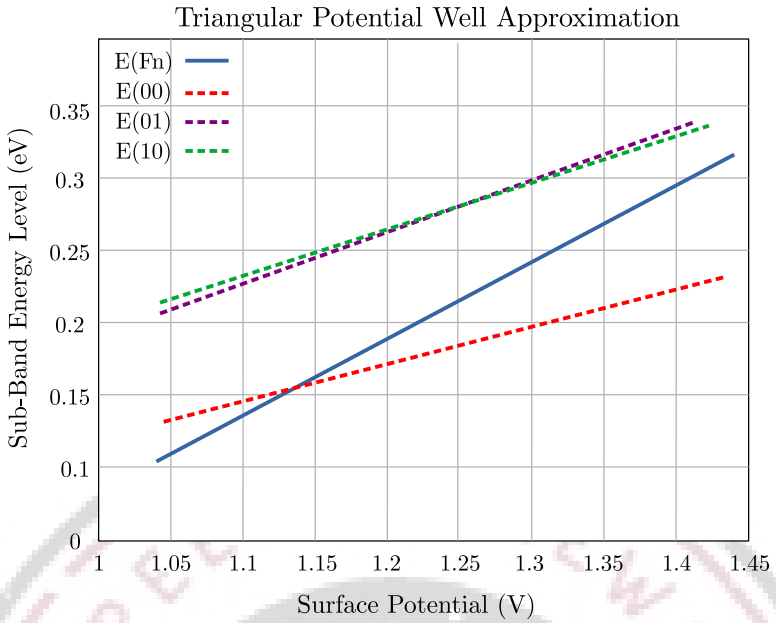

Figure 6: Triangular Potential Well Approximation for First Three Quantized Energy Levels and Quasi-Fermi Level versus Surface Potential

In this figure, what is also shown in the quasi-Fermi level at the surface E_{F_n}. As the surface potential, ϕ_S, increases, all three sub-band levels increases, along with the quasi-Fermi level. When the surface potential reaches around 1.2 V, the quasi-Fermi level surpasses the lowest sub-band E_{00}. As the surface potential get larger, the difference between the subband levels, especially between E_{00} and the other two levels are increased, indicating a more severe energy band splitting when the electric field is increased.

The carrier density located at each energy level (N_{00}, N_{01} and N_{10}) versus the surface potential is shown in Figure 7. Most of the carrier are located in the lowest energy sub-band E_{00}. As the surface potential increases and the surface is more inverted, there are more minority carriers in the channel area. N 00 grows the fasted with the surface potential. A more intuitive representation of such trend, where the composition of the total inversion carrier density is shown. As the surface electric field increase and the total inversion carrier density get larger, more and more carriers are located in the lowest sub-band E_{00}. Over the range where the later simulation is conducted, more than 80% of the inversion layer carriers are located in E_{00}.

However, if one can find a reasonable approximation of the energy levels for the holes in the inversion layer in PMOS transistors, plus the careful choice of parameters for holes, such as effective mass, density of state etc., the rest of the noise simulation employed in this work can be easily adopted for PMOS. Most of the carriers are located in the lowest sub-band E_{00}. As the surface potential get larger, the surface become more "inverted". The model presented in this work can also be applied to materials besides Si. For each material and device system, with the careful construction of energy band and sub-band structures and appropriate choice for physical parameters of the corresponding materials, one can easily employ this modified unified $1/f$ noise model to model and predict the $1/f$ noise behavior of the device under test.

VI Conclusion

This paper offers a triangular potential well approximation in scaled MOSFET for $1/f$ low frequency noise modeling and characterization in nano-scaled MOS devices. The simulation based on the proposed model shows good agreement with the experimental results obtained from a high-K NMOS transistor with ultra-thin oxide. It addressed the modeling and characterization of scaled silicon CMOS devices. This paper presented research on channel implantation on advanced replacement gate technology as a cost-effective approach to precisely control the channel dopant profile in the next-generation CMOS technology. In addition, this research suggest some recommendations for future work of nanoscaled CMOS devices. The triangular well approximation replaces the potential in Schrödinger and Poisson equations inside the silicon substrate and by an infinite barrier in the dielectric based on the assumption of a linear shape of the potential in the semiconductor surface layer.

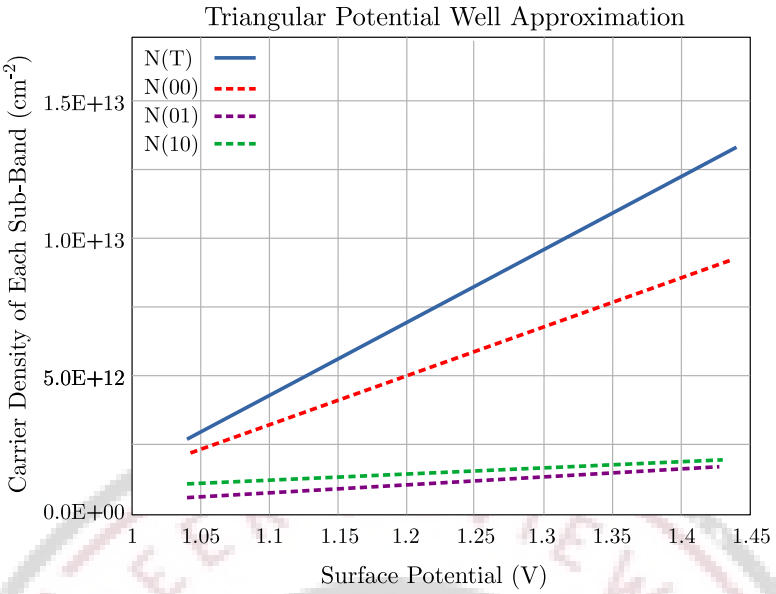

Figure 7: Triangular Potential Well Approximation for Inversion Layer Carrier Density versus Surface Potential

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