Implementation of CMOS Based SRAM Memory

MD NAEEM[1], DR. LAXMI SINGH[2]
[1] M.Tech Student, Department of Electronics and Communication Engineering, RNTU, Bhopal
[2] Associate Professor, Department of Electronics and Communication Engineering, RNTU, Bhopal

* Corresponding Author: MD Naeem

Abstract: ***Low power static-random access memories (SRAM) has become a critical component in modern VLSI systems. In cells, the bit-lines are the most power consuming components because of larger power dissipation in driving long bit-line with large capacitance. The cache write consumes considerable large power due to full voltage swing on the bit-line. The aim of the paper is to propose a new SRAM cell architecture to reduce the power consumption during write 0 and write 1 operation. The paper proposes a SRAM cell to reduce the power in write "0" as well as write "1"operation by introducing two tail transistors. The SRAM cell consumes less power than the conventional SRAM cell during write operation. The write access delay is reported to be lower than conventional. The Proposed SRAM cell designed and implemented with using .0.18µm CMOS technology. Simulation is performed by Microwind 3.1 software. We design a 64-bits memory with the help of SRAM cell. The power dissipated in Proposed SRAM memory is reduced up to 18.88% in comparison to Conventional SRAM memory***.
Keywords:.. CMOS, Dynamic Power, SRAM, Threshold Voltage, leakage current, VLSI.

I. Introduction

Power consumption in SRAM cell is considered one of the most important problems on high performance chips due the popularity of battery operated electronic devices and mobile devices According to research done, the power dissipated in the bit lines represents about 68% of total dynamic power consumption during a write operation only. Therefore, most of the research work is focuses on the power reduction during write operation. For reducing the power consumption in SRAM cell, different kinds of architectures from 5-transistor to 17-transistor for SRAM cell was given in different papers. One of the oldest techniques is Zero- Aware (ZA) asymmetric Cell for reducing the dynamic power consumption. Another method is Low power 7T SRAM Cell for reducing the static power dissipation. Since, most power consumption comes from discharging of the bit lines; a 5T cell utilizing a single bit line for read/write operation has also been designed. Another common method is to use boosted word line technique to improve the write operation, however this incurs external circuitry and cell instability. Virtual grounding is a well-known technique to reduce the WRITE power consumption . The cells are based on the Vt-control of the cross-coupled inverters of the SRAM cell to reduce leakage power when SRAM is in the idle mode. The other technique is Low Power SRAM Design using Charge Sharing Technique. In this method a low-power write scheme by adopting charge sharing technique. By reducing the bit-lines voltage swing, the bit-lines dynamic power is reduced. Another method is hierarchical divided bit-line approach for reducing active power in SRAMs by reducing bit-line capacitance. During read or write mode at least one of the tail transistor must be turned OFF to disconnect the driving path of respective inverters. These transistors also reduce the sub threshold current during transistor OFF condition.

II. CONVENTIONAL SRAM CELL

Figure 1 shows the schmatic of conventional SRAM cell.

A. WRITE CYCLE - Values 1 or 0 must be placed on Bit Line, and the data inverted value on ~Bit Line. Then the selection Word Line goes to 1. The two-inverter latch takes the Bit Line value. When the selection Word Line returns to 0, the RAM is in a memory state.

B. READ CYCLE - The selection signal Word Line must be asserted, but no information should be imposed on the bit lines. In that case, the stored data value propagates to Bit Line, and its inverted value ~Data propagates to ~Bit Line.

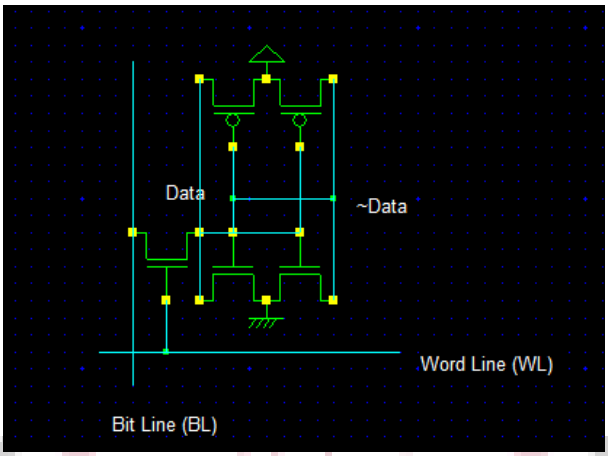


Figure 1 : Design of 5T SRAM Cell

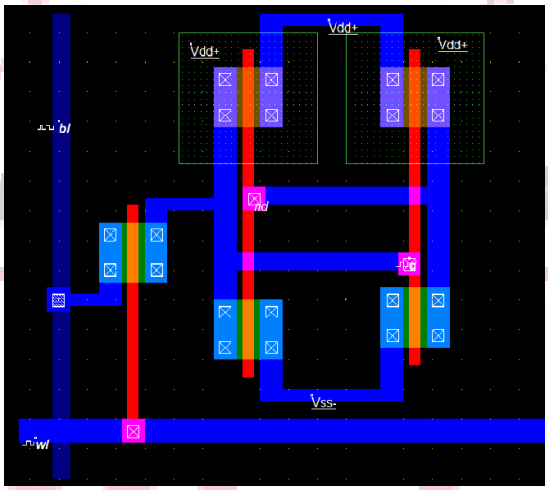


Figure 2 : Design of 5T SRAM Cell

(MICROWIND3.1)

C. SIMULATION - The simulation parameters correspond to the read and write cycle in the SRAM. The proposed simulation steps consist in writing a 0, a 1, and then reading the 1. In a second phase, we write a 1, a 0, and read the 0. The Bit Line and ~Bit Line signals are controlled by pulses . The floating state is obtained by inserting the letter "x" instead of 1 or 0 in the description of the signal.

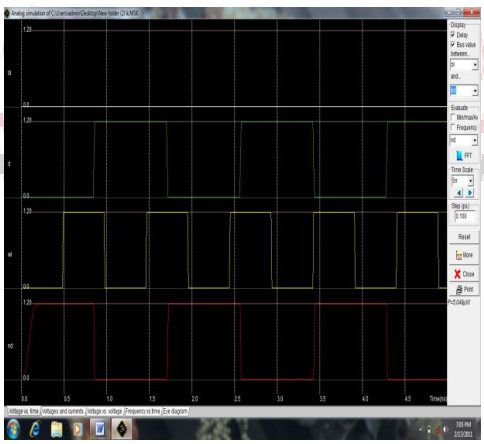
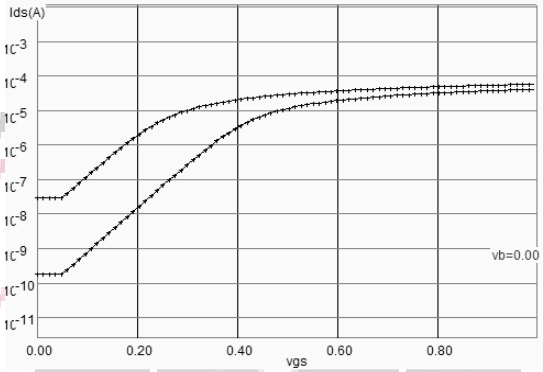


Figure 3 : Simulation of a 5T SRAM

Cell (Microwind3.1)

III. LOW LEAKAGE EFFECT

A new kind of MOS device has been introduced in deep submicron technologies, starting the 0.18µm CMOS process generation. The new MOS, called high speed MOS (HS) is available as well as the normal one, recalled Low leakage MOS (LL). The main objective is to propose two types of devices, one which reduces significantly the leakage current (LL version), that is the small current Ioff that flows from between drain and source with a gate voltage 0 (Supposed to be no current in first order approximation). The low leakage MOS device (right side) has an Ioff current reduced by a factor 100, thanks to a higher threshold voltage (0.4V rather than 0.3V).



100 times less leakage Ioff

Fig. 4: Low leakage for lower Ioff Current

The main drawback of the Low leakage MOS device is a 30% reduction of the Ion current, leading to a slower switching. High speed MOS devices should be used in the case of fast operation linked to critical nodes, while low leakage MOS should be placed whenever possible, for all nodes where a maximum switching speed is not required.

Temperature effects

Three main parameters are concerned by the sensitivity to temperature: the threshold voltage VTO, the mobility U0 and the slope in sub-threshold mode. Both VTO and U0 decrease when the temperature increases.

In Microwind 3.1, TNOM is fixed to 300°K, equivalent to 27°C. UTE is negative, and set to -1.8 in 0.12µm CMOS technology, while KT1 is setto -0.06 by default . A higher temperature leads to a reduced mobility, as UTE is negative. Consequently, at a higher temperature, the current Ids is lowered.

IV. SRAM OPERATION

A. Design

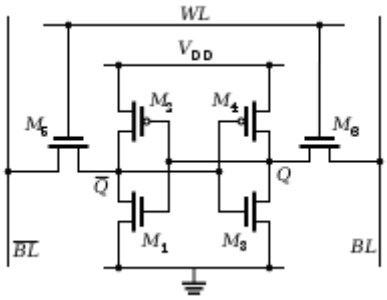


Fig. 5: A six-transistor CMOS SRAM cell.

An SRAM cell has three different states it can be in: standby where the circuit is idle, reading when the data has been requested and writing when updating the contents. The three different states work as follows:

B. Standby

If the word line is not asserted, the access transistors M5 and M6 disconnect the cell from the bit lines. The two cross coupled inverters formed by M1 – M4 will continue to reinforce each other as long as they are connected to the supply.

C. Reading

Assume that the content of the memory is a 1, stored at Q. The read cycle is started by precharging both the bit lines to a logical 1, then asserting the word line WL, enabling both the access transistors. The second step occurs when the values stored in Q and Q are transferred to the bit lines by leaving BL at its precharged value and discharging BL through M1 and M5 to a logical 0. On the BL side, the transistors M4 and M6 pull the bit line toward VDD, a logical 1. If the content of the memory were a 0, the opposite would happen and BL would be pulled toward 1 and BL toward 0.

D. Writing

The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL to 1 and BL to 0. This is similar to applying a reset pulse to a SR-latch, which causes the flip flop to change state. A 1 is written by inverting the values of the bit lines. WL is then asserted and the value that is to be stored is latched in. Note that the reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters. Careful sizing of the transistors in an SRAM cell is needed to ensure proper operation.

E. Bus behavior

A RAM memory with an access time of 70 ns will output valid data within 70 ns from the time that the address lines are valid. But the data will remain for a hold time as well (5-10 ns). Rise and fall times also influence valid timeslots with approximately ~5 ns. By reading the lower part of an address range bits in sequence (page cycle) one can read with significantly shorter access time (30 ns).

F. Characteristics

SRAM is more expensive, but faster and significantly less power hungry (especially idle) than DRAM. It is therefore used where either bandwidth or low power, or both, are principal considerations. SRAM is also easier to control (interface to) and generally more truly random access than modern types of DRAM. Due to a more complex internal structure, SRAM is less dense than DRAM and is therefore not used for high-capacity, low-cost applications such as the main memory in personal computers.

G. Clock rate and power

The power consumption of SRAM varies widely depending on how frequently it is accessed; it can be as power-hungry as dynamic RAM, when used at high frequencies, and some ICs can consume many watts at full bandwidth. On the other hand, static RAM used at a somewhat slower pace, such as in applications with

moderately clocked microprocessors, draw very little power and can have a nearly negligible power consumption when sitting idle — in the region of a few micro-watts.

H. Uses

Static RAM exists primarily as:

A. general purpose products
- with asynchronous interface, such as the 28 pin 32Kx8 chips (usually named XXC256), and similar products up to 16 Mbit per chip
- with synchronous interface, usually used for caches and other applications requiring burst transfers, up to 18 Mbit (256Kx72) per chip

B. integrated on chip
- as RAM or cache memory in micro-controllers (usually from around 32 bytes up to 128 kilobytes)
- as the primary caches in powerful microprocessors, such as the x86 family, and many others (from 8 kB, up to several megabytes)
- to store the registers and parts of the state-machines used in some microprocessors -- see register file
- on application specific ICs, or ASICs (usually in the order of kilobytes)
- in FPGAs and CPLDs (usually in the order of a few kilobytes or less

V. RESULTS & DISCUSSION

This section provides the detailed simulation analysis of the 64-bit SRAM cell. We estimate the impact of the SRAM cell on the power dissipation during write operation. The schematic of SRAM cell is designed and implemented by using Microwind. The design has been simulated using CMOS .12µm technology. Then we design a 64-bits memory by using SRAM cell and the result is compared with Conventional 5-T SRAM cell. The two stack transistors reduce dynamic power consumption during write operation through proper charging and discharging of the bit lines. In the conventional SRAM cell, one of the two bit lines must be discharged to low regardless of written value, therefore the power dissipation in both write "0" and "1" is more. In our SRAM cell as shown in figure 2, we are preventing any single bit line from being discharged during write "0" as well as write "1" mode by proper selection of control signal .We design a Layout of the SRAM cell by using Microwind Layout Design Tool. The Layout of SRAM has been shown in figure 6. The layout is based on λ- Design Rules, where λ is equal to the Half of the length of the transistor used in standard foundry that is.0.18µm.

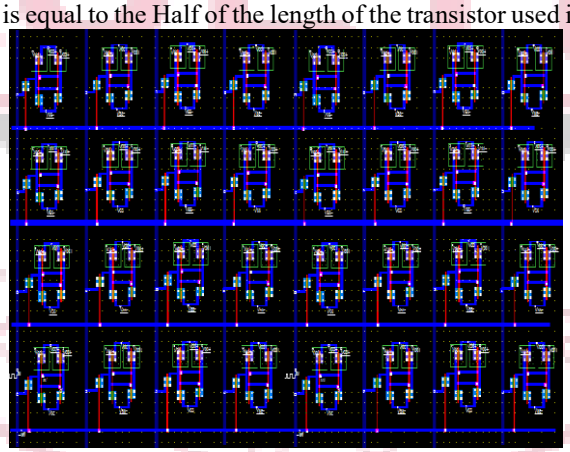


Figure 6. Layout of 64-bit SRAM cell

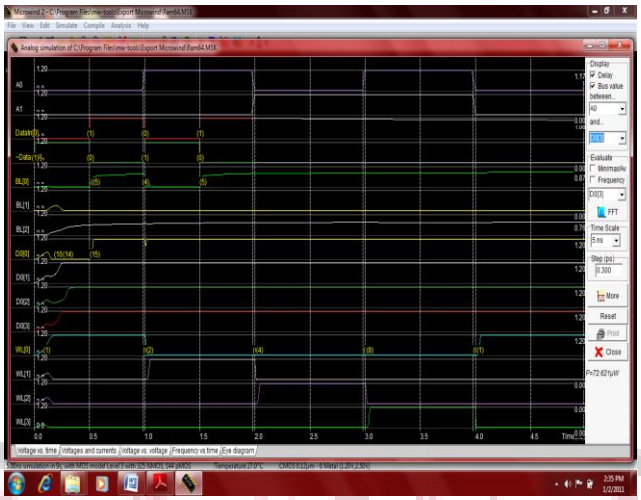


Figure 7: Simulation 64-bit SRAM cell

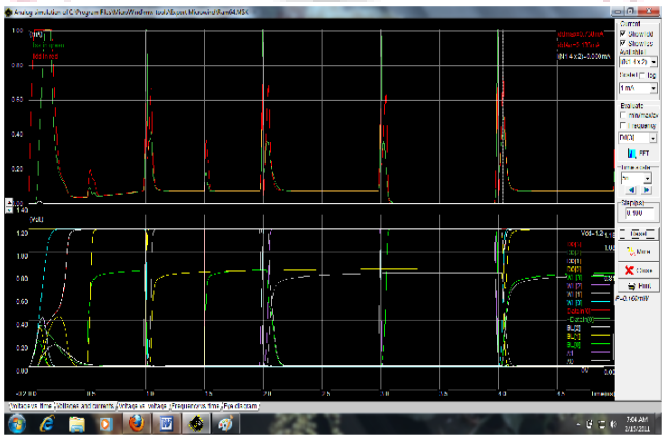


Figure 8: Voltage vs Current Graph

VI. CONCLUSION & FUTURE WORK

Most of the developed low-power SRAM techniques are used to reduce only read power. Since, in the SRAM cell, the write power is generally larger than read power. But here SRAM cell can reduce the power in write operation by introducing two tail Transistors in the Pulldown path for reducing leakages. Due to these Stack transistors the power dissipation has reduced up to 19.83% for a single SRAM cell and 18.88% for 64-bits memory in comparison to Conventional 6T SRAM. Although number of transistors are increased but relative power dissipation is also be reduced. In future work we will design area efficient Proposed SRAM memory with the help of Layout Design Techniques. This SRAM cell can be used to provide low power and low cost solution for portable devices like laptops, mobile phones etc

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