

Review of Existing Techniques for Enhanced Stability and Efficiency

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Abstract:-This work presents the performance optimization of a CMOS ring oscillator using different multi-objective optimization algorithms: Multi-Objective Particle Swarm Optimization (MOPSO), Multi-Objective Grey Wolf Optimizer (MOGWO), and Multi-Objective Cuckoo Search (MOCS). The performance metrics considered are the oscillator's frequency, power consumption, phase noise at a 1 MHz offset, and the figure of merit.

Keywords:- Power Amplifier, Optimization, Multi-Objective, Cuckoo Search, Grey Wolf Optimizer

1. Introduction

CMOS ring oscillators are essential components in integrated circuit design due to their simplicity and versatility. They are crucial in digital, analog, and mixed-signal circuits. Their unique setup generates periodic waveforms, essential for applications like clock generation, frequency synthesis, delay generation, and BIST functions. CMOS ring oscillators integrate seamlessly into large-scale ICs, promoting cost-effectiveness and design simplicity. A CMOS ring oscillator is a series of CMOS inverters, each with a PMOS and NMOS transistor, connected in a closed loop [1]. This configuration generates an oscillating signal by continuously inverting the input signal and propagating it through the stages. The frequency of the oscillation is determined by the delay introduced by each inverter stage, with the total oscillation period being twice the cumulative propagation delay of all the stages. An odd number of stages is essential for the correct phase shift for sustained oscillation. CMOS ring oscillators are fundamental building blocks in modern digital and analog integrated circuits, playing a crucial role in various applications, including clock generation, frequency synthesis, and delay generation. Their simplicity, low power consumption, high noise immunity, and scalability make them cost-effective and suitable for large-scale integration. Ring oscillators are crucial in phase-locked loops (PLLs) for frequency synthesis, testing, characterization, power management, and temperature sensing [2]. They provide precise control over clock frequencies, optimize timing performance, and characterize manufacturing processes. Their sensitivity to process variations ensures ICs meet performance criteria. CMOS ring oscillators are indispensable tools in modern electronics, contributing to reliable and efficient IC designs. Ring oscillators are crucial in power management strategies like dynamic voltage and frequency scaling (DVFS) and temperature sensing, maintaining circuit stability. Their simplicity and effectiveness make them indispensable in modern electronics, contributing to reliable and efficient IC designs. As demand for efficient, reliable, and compact electronic systems grows, CMOS ring oscillators continue to drive innovation [3]. CMOS ring oscillators are crucial in integrated circuit (IC) design due to their versatility and critical role in ensuring the functionality and performance of ICs. These oscillators consist of an odd number of inverters connected in a loop, producing a periodic oscillating signal. They are essential for generating precise clock signals, synchronizing digital circuits, and ensuring reliable operation of complex systems. They also serve as critical delay elements in testing and characterization. Their low power consumption, high noise immunity, and robustness against process variations make them suitable for various applications, including IoT, wearable electronics, and biomedical devices [4].

2. Literature Review

A novel sizing technique to improve the efficiency and performance of CMOS ring oscillators (ROs) is presented by Mohammadi et al. [1]. This approach balances several design objectives by using circuit simulation and multi-objective optimisation techniques. Power consumption, phase noise, figure of merit, integration index, design cycle time, and Pareto front concerns are all taken into account while estimating circuit characteristics. Four optimisation strategies are used in the study to attain the best outcomes in 0.18- μm CMOS technology.

A novel design with four static single-ended inverters and four feedforward inverters is proposed by Grozing et al. [2]. This topology improves phase noise and lowers quadrature error.

Sikarwar et al. [3] describe the design and analysis of a nine-stage ring oscillator using the Cadence Virtuoso tool in 45 nm technology. Their design aims to minimize power consumption, jitter, noise, and periodic steady-state response, achieving an 18.9% reduction in power consumption.

Jalil et al. [4] explore the implementation techniques and performance comparisons of the Differential Ring Oscillator (DRO) as a CMOS voltage-controlled oscillator (VCO) in low radio frequency (RF) bands. The study discusses various circuit approaches and their performance.

Mandal et al. [5] examine the structure and operating principles of ring oscillators (RO), focusing on the frequency of oscillation and propagation delay of delay stages. The study addresses techniques to overcome limitations, such as negative skewed delay RO, multi-feedback RO, and coupled RO. It also discusses potential applications based on voltage tuning characteristics and multiphase outputs.

Fortuny et al. [6] investigate ring oscillator (RO)-based degradation and annealing monitors on a 28 nm versatile array chip. The test vehicle enables reliable statistical characterization of RO monitor circuits stressed by BTI and HCD, as well as their annealing behavior, providing detailed insights into their performance.

Corradini et al. [7] introduce a rapid simulation-based method for characterizing CMOS ring oscillators (ROs), essential for energy management in self-powered systems. This method extracts key parameters from AC simulations of the unitary-stage CMOS inverter, allowing for the estimation of dynamic behavior using analytical expressions rather than extensive transient simulations.

Gate et al. [8] present a voltage-controlled ring oscillator (VCRO) utilizing a carbon nanotube field-effect transistor (CNTFET). The design features a delay cell based on a three-transistor NAND gate, with VCO circuits configured in three, five, and seven stages. Simulations indicate that oscillation frequencies range from 274.56 GHz to 348.29 GHz, with power consumption between 92.49 μ W and 120.96 μ W. The power delay product (PDP) is evaluated as a figure of merit, making this design suitable for low power and extremely high-frequency applications.

Sadeghi et al. [9] propose a temperature-compensated ring oscillator designed for low power consumption in bio-implantable and wearable devices. While conventional ring oscillators are apt for biomedical applications, their frequency is temperature-dependent. The proposed design employs two current sources, one temperature-independent and the other complementary to absolute temperature (CTAT), to power the subthreshold ring oscillator. This approach reduces the ring oscillator's thermal coefficient to 80.4 ppm/ $^{\circ}$ C, achieving a total power consumption of only 14.5 μ W.

Luo et al. [10] describe an energy-efficient true random number generator (TRNG) that leverages the jitter noise of a single ring oscillator (RO). This TRNG generates consecutive pulses due to the fixed intrinsic propagation delay and time-varying jitter noise. The design, fabricated using a 40-nm standard CMOS process, demonstrates high energy efficiency of 2.5 pJ/bit at 53 Mbps, and its randomness is validated through characterization.

3. Methodology

A ring oscillator (RO) is an active electrical device known as a complementary metal-oxide-semiconductor (CMOS) consisting of an odd number of NOT gates (inverters) linked in a loop. In a CMOS ring oscillator (RO), inverters are the main components consuming power. The total power consumption is divided into static and dynamic components. Static power, caused by leakage current, is negligible. Dynamic power results from short circuit (crowbar) current and switching current. The total power consumption of the RO circuit can be calculated by considering these dynamic power contributions:

$$Power = \frac{W}{L}, \frac{V_{DD}^2 (V_{DD} - V_T)^2}{2 \cdot (V_{DD} - 2V_T) \left(\frac{1}{K_{pp}} + \frac{1}{K_{pn}} \right)} \quad (1)$$

Phase noise is a continuous stochastic process that reflects random variations in the phase of an oscillator operating at a steady frequency. It is primarily caused by white noise, control voltage noise, and flicker noise. The total phase noise of the circuit can be expressed by considering these contributing factors:

$$L\{\Delta f\} = \frac{8 kT V_{DD} f_{osc}^2}{3\eta P V_{char} \Delta f^2} \quad (2)$$

$$V_{char} = \Delta V / \gamma \quad (3)$$

In Eqs. (2) and (3), f is the offset frequency from the carrier at which the phase noise is measured, V is the gate over drive voltage, K is Boltzmann constant, T is absolute temperature, and γ is a coefficient which is 2/3 for long channel devices in saturation Hajimiri et al. (1999). The FoM is a quality performance measure of a RO and is defined in the form of Eq. (4).

$$F_0M = 10 \log_{10} \left[L\{\Delta f\} \frac{\Delta f^2}{f_{osc}^2} \frac{P}{1mw} \right] \quad (4)$$

Optimization of CMOS RO

This section describes the proposed approach for optimizing and enhancing the performance of a CMOS ring oscillator (RO). Recent research has explored numerous optimization techniques to find the best solutions for various practical problems. In this section, a simulation-based optimization tool is used to solve the optimal design problem of the proposed CMOS RO circuit. This approach bypasses the traditional modeling stage and directly uses a simulator to evaluate objective or fitness functions and check circuit constraints, as shown in Figure 1.

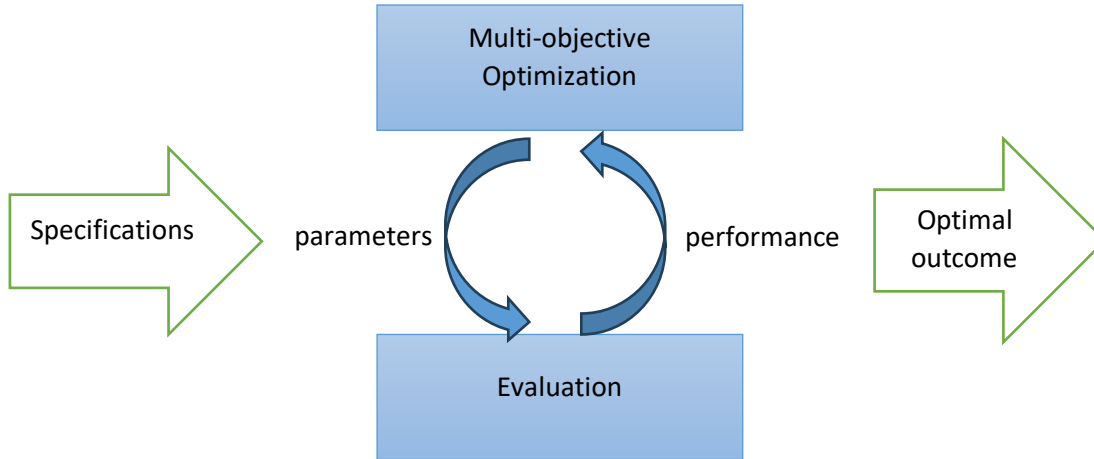


Figure 1: Simulation-based sizing/optimizing tool

4. Performance Measures

Here are the definitions and mathematical equations for the performance parameters used in the CMOS ring oscillator design optimization:

Frequency (f_{out}): The frequency of the ring oscillator, which determines how fast the oscillator operates

$$f_{out} = \frac{1}{2 \cdot N \cdot t_{delay}} \quad (5)$$

Where N is the number of stages in the ring oscillator, and t_{delay} is the propagation delay of each stage.

Power Consumption: The total power consumed by the ring oscillator.

$$P = V_{dd}^2 * f_{out} * C_{load} \quad (6)$$

where V_{dd} is the supply voltage, f_{out} is the frequency, and C_{load} is the load capacitance.

Phase Noise: The phase noise of the oscillator measured at a 1 MHz offset from the carrier frequency. It indicates the purity of the signal in the frequency domain.

$$L(f_m) = 10 \log_{10} \left(\frac{1}{2} \left(\frac{f_{out}}{f_m} \right)^2 \frac{kT}{P} \right) \quad (7)$$

where f_m is the offset frequency (1 MHz), k is Boltzmann's constant, T is the absolute temperature, and P is the power consumed by the oscillator.

Figure of Merit (FoM): A comprehensive performance metric that combines frequency, power consumption, and phase noise.

$$FoM = L(f_m) + 10 \log_{10} \left(\frac{f_{out}}{P} \right) \quad (8)$$

where $L(f_m)$ is the phase noise at a 1 MHz offset, f_{out} is the frequency, and P is the power consumption.

5. Conclusion and Future Scope

This study provides valuable insights for designers to make informed decisions in optimizing CMOS ring oscillators for diverse applications. Future research can explore the integration of hybrid optimization techniques that combine the strengths of different algorithms to achieve even better performance for CMOS ring oscillators. Additionally, extending the study to include more advanced and emerging algorithms such as Quantum-inspired algorithms or machine learning-based optimization methods could provide further improvements in design efficiency and performance. Investigating the impact of process variations and environmental factors on the optimized designs could enhance the robustness and reliability of the oscillators. Furthermore, applying these optimization techniques to other types of oscillators and analog circuits can broaden the applicability and benefits of multi-objective optimization in electronic design automation.

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